IN THE CLAIMS

This listing of the claim will replace all prior versions and listings of claim in the present application.

Listing of Claims

1. (currently amended)A communication apparatus ~~switching system~~ for interconnecting plural kinds of communication networks including an asynchronous transfer mode (ATM) network to transfer information,~~and transferring information among the networks,~~ said communication apparatus comprising:

plural kinds of first interfaces for converting plural kinds of control signals or communication signals from ~~the~~ plural kinds of communication networks, except the ATM network, to ATM ~~into asynchronous transfer mode~~ cells ~~(ATM cells)~~;

a second interface for receiving an ATM cell to which a control signal or a communication signal is inserted from the ATM network;

an ATM switch having a plurality ~~pluralities~~ of input ports and a plurality of output ~~lines~~ ports for outputting an ~~transferring an~~ ATM cell received by any one of the input ports from the first and second interfaces ~~lines from one of the interfaces~~ to any one of the plurality of output ~~lines~~ports based on header information of the ATM cell;~~and~~

plural kinds of signal processors, connected to the ATM switch, for converting a signal output from the first and second interfaces to a signal format or protocol used by each of the plural kinds of communication networks; and~~, each of which converts control information outputted from one of the interfaces into a signal format, alternatively a protocol, used by each of the plural kinds of communication networks.~~

a control part for receiving the ATM cell, which is output from one of the plural kinds of signal processors and to which a control signal is inserted through the ATM switch, and performing a necessary processing among plural kinds of processing.

Claim 2 (canceled).

3. (currently amended)A communication apparatus ~~switching system~~ according to claim 1~~2~~, wherein said control processor includes plural kinds of processors for executing different processing, and a second ATM switch connected to one of plural kinds of processors for transferring inter-processor information to the other processor as a destination based on header information of an ATM cell,

said processor outputs an ATM cell having a header destined to the other processor performing necessary control to the second ATM switch, and said second ATM switch transmits the ATM cell to the other processor as a destination.

a2 cont

4. (currently amended)A communication apparatus ~~switching system~~ according to claim 1, wherein each of said signal processors forms an ATM cell having a header destined to any one of the control part, the first interfaces and the second interface~~processors, alternatively the interfaces~~, and outputs the ATM cell.

5. (currently amended)A communication apparatus switching system according to claim 1, wherein each of said signal processors relays an IP packet converted into an ATM cell among the plural kinds of communication networks.

6. (currently amended)A communication apparatus switching system according to claim 1, wherein each of said signal processors converts the ATM cell based on a signal received through a common line, and then outputs the cell to one of the communication networks.

Claim 7 (canceled).

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8. (currently amended)A communication apparatus switching system according to claim 1, wherein each said first and second interfaces converts control signal ~~information~~ received from one of the communication networks into an ATM cell having a header destined to any one of the signal processors for performing signal processing, and outputs the ATM cell to the ATM switch.

Claims 9-17 (canceled).